IN THE CLAIMS

Please amend the claims to be in the form as follows:

Claim 1 (currently amended): A multi-processor unit ~~(100)~~, comprising: communication means ~~(101, 102)~~ for receiving data into the unit, transmitting data from the unit; first domain processing means ~~(103)~~ for first processing the data depending on first domain configuration information, the first domain processing means including multiple first domain processors ~~(105-108)~~ each connected to the communication means for receiving data and transmitting data to the communication means including data transmitted between processors, each first domain processor differently sub-processing the data in order to first process the data, the first domain processors including a first domain control processor ~~(105)~~ for controlling the first processing of the first domain; second domain processing means ~~(110)~~ for second processing the first processed data depending on second domain configuration information, the second processing being different than the first processing, the second domain processing means including multiple second domain processors ~~(111-115)~~ each connected to the communication means for receiving data and transmitting data to the communication means including data transmitted between processors, each second domain processor differently sub-processing the data in order to second process the data, the second domain processors including a second domain control processor ~~(111)~~ for controlling the second processing of the second domain; and a global control processor ~~(120)~~ connected to the communication means for providing the first domain configuration information and the second domain configuration information through the communication means for configuring the first and second domains.

Claim 2 (currently amended): The multi-processor unit of claim 1, in which: the communication means include a stream-based communication means ~~(101)~~ connected to the global control processor and connected to a plurality of the processors of the first and second domains including the first and second domain control processors for transmitting information streams between the connected processors; the stream-based communications

means are connected to an input/output bus ~~(120)~~ to at times receive a stream of data into the multi-processor unit through the stream-based communications means into one of the connected processors and to at other times transmit a stream of data from one of the connected processors through the stream-based communications means onto the input/output bus; the multi-processor unit includes blocks ~~(130-136)~~ of electronic memory ~~(137)~~ and the communication means includes block-based communication means ~~(138)~~ connected to the memory blocks and connected to one or more of the first domain processors and one or more of the second domain processors for selectively interconnecting the connected processors to the memory blocks, with only one processor at a time being interconnected to one of the memory blocks, and processors of different domains being interconnected at different times to the same memory block; the control of the domain control processors during operation includes data flow driven control so that receiving a data object through the stream-based communication means triggers processing by the domain control processor; the data objects include data and indicators of memory blocks, when a domain receives an indicator of a memory block it has exclusive access to the memory block and when the domain passes the indicator of the memory block it yields all access to the memory block; the indicators of memory blocks include addresses of the memory blocks; each domain control processor, controls access between the memory blocks that the domain has exclusive access to and the processors of the domain; each processor that is connected to the block-based communication means receives data from the memory blocks and stores data in the memory blocks through address and data registers ~~(140-145)~~ of the processor and control signals from the domain control processor control operations of the registers of the processors of the domain that load and store information to the memory blocks exclusively accessed by the domain; within the domains, control of the processors includes data flow driven control depending on data received by the processor from the stream-based communication means and from the memory blocks through the registers controlled by the domain control processor; within the domains, control of the processors includes direct control by the domain control processor by control signals provided directly through control lines ~~(150, 151)~~ to the other domain processors from the domain control processor; at least one of the domain control processors includes a periodic sequencer that initiates control commands

transmitted to other processors to initiate subroutines in those processors depending on an index counter; the processing of the first domain including FFT and IFFT processing of blocks of data in the memory blocks; the processing of the second domain including equalization of blocks of data in the memory blocks; the multi-processor unit further comprises a third domain processing means ~~(160)~~ including at least one processor ~~(161)~~ connected to the stream-based communication means for forward error correction of a stream of data; each processor is structurally different from the other processors of the multi-processor unit for performing a different portion of channel decoding of transmission signals; the first and second domain configuration information configures the domains for channel decoding transmissions based on different modulation standards; the configuration information provided by the global control processor at times configures the first domain processing means and the second domain processing means for channel decoding 8-VSB transmissions based on the ATSC standard; the configuration information provided by the global control processor at other times configures the first domain processing means and the second domain processing means for channel decoding COFDM transmissions based on the DVB-T standard.

Claim 3 (currently amended): An integrated circuit chip ~~(300)~~ containing the multi-processor unit ~~(100)~~ of claim 1, comprising: a substrate ~~(301)~~ of semiconductor material with different portions having different levels of impurities; and a layer of insulation ~~(302, 303)~~ on the semiconductor substrate; a layer of wiring ~~(304, 305)~~ including connection pads ~~(306, 307)~~ for flip-chip or wire-bond connection to a circuit board; and wherein the different portions of semiconductor material and wiring layer provide the multi-processor unit ~~(100)~~ of claim 1.

Claim 4 (currently amended): A circuit board assembly ~~(310)~~ including the integrated circuit chip of claim 3, comprising: a circuit board substrate ~~(311)~~; a wiring layer ~~(312)~~ on the circuit board substrate including connection pads for an integrated circuit chip; the integrated circuit chip ~~(300)~~ of claim 3 mounted on the circuit board substrate; and flip-chip or wire-bond connections ~~(313, 314)~~ between the connection pads of the integrated circuit chip and the connection pads of the wiring layer.

Claim 5 (currently amended): A set-top-box ~~(320)~~ containing the circuit board assembly ~~(310)~~ of claim 4, comprising: a connection ~~(321)~~ for receiving a channel encoded multimedia signal; a connection ~~(322)~~ for transmitting a channel decoded multimedia signal; the circuit board assembly ~~(310)~~ of claim 4 for decoding the encoded multimedia signal to provide the decoded multimedia signal; and a power supply ~~(323)~~ connected to the circuit board assembly to provide power.

Claim 6 (currently amended): A digital television set ~~(330)~~ containing the circuit board assembly ~~(310)~~ of claim 4, comprising: a source ~~(331)~~ for providing a channel encoded multimedia signal from a transmission media; the circuit board assembly ~~(310)~~ of claim 4, for decoding the encoded multimedia signal to provide a decoded multimedia signal; a power supply ~~(332)~~ connected to the circuit board assembly to provide power to the circuit board assembly; a display ~~(333)~~ connected to the circuit board assembly for presenting the video signals of the decoded multimedia signal; and a connection ~~(334)~~ for a load speaker ~~(335)~~ for presenting audio signals of the decoded multimedia signal.

Claim 7 (original): A multi-processor system for processing data, comprising: a plurality of memory blocks in an electronic memory; block-based communication means connected to the memory blocks to provide access to the memory blocks; stream-based communication means; a plurality of processors connected to the block-based communication means for processing data in the memory blocks and connected to the stream-based communication means for providing data objects from a processor to a subsequent processor, the data objects including data for processing the data and pointers to memory blocks to control access to the memory blocks, the processors having means for data flow driven process control so that receiving data objects from a previous processor through the stream-based communication means triggers processing by the subsequent processor that receives those data objects, each processor having exclusive control for accessing data in one or more of the memory blocks, and each processor receiving the exclusive control of a memory block by receiving the pointer to the memory block from the previous processor through the stream-based communications means and

each processor yielding exclusive control to the subsequent processor by providing a pointer to the memory block to the subsequent processor through the stream-based communication means.

Claim 8 (new): The multi-processor system of claim 7, wherein the communication means perform block-based communication with the memory blocks and connect to one or more of the first domain processors and one or more of the second domain processors for selectively interconnecting the connected processors to the memory blocks, with only one processor at a time being interconnected to one of the memory blocks, and processors of different domains being interconnected at different times to the same memory block.

Claim 9 (new): The multi-processor system of claim 7, wherein the control of the domain control processors during operation includes data flow driven control so that receiving a data object through the stream-based communication means triggers processing by the domain control processor.

Claim 10 (new): The multi-processor unit of system 7, wherein control of the domains by the domain control processor is provided directly through control lines to the other domain processors from the domain control processor.

Claim 11 (new): The multi-processor unit of system 7, wherein each processor is structurally different from the other processors of the multi-processor unit for performing a different portion of channel decoding of transmission signals.

Claim 12 (new): The multi-processor unit of system 7, wherein the first and second domain configuration information configures the domains for channel decoding transmissions based on different modulation standards.

Claim 13 (new): The multi-processor unit of system 7, wherein the configuration information provided by the global control processor at times configures the first domain

processing means and the second domain processing means for channel decoding 8-VSB transmissions based on the ATSC standard.

Claim 14 (new): The multi-processor system of claim 7, wherein the configuration information provided by the global control processor at other times configures the first domain processing means and the second domain processing means for channel decoding COFDM transmissions based on the DVB-T standard.

Claim 15 (new): The multi-processor system of claim 1,wherein the multi-processor unit includes blocks of electronic memory and the communication means perform block-based communication with the memory blocks and connected to one or more of the first domain processors and one or more of the second domain processors for selectively interconnecting the connected processors to the memory blocks, with only one processor at a time being interconnected to one of the memory blocks, and processors of different domains being interconnected at different times to the same memory block.

Claim 16 (new): The multi-processor system of claim 1, wherein the control of the domain control processors during operation includes data flow driven control so that receiving a data object through the stream-based communication means triggers processing by the domain control processor.

Claim 17 (new): The multi-processor system of claim 1, wherein control of the domains by the domain control processor is provided directly through control lines to the other domain processors from the domain control processor.

Claim 18 (new): The multi-processor system of claim 1, wherein each processor is structurally different from the other processors of the multi-processor unit for performing a different portion of channel decoding of transmission signals.

Claim 19 (new): The multi-processor system of claim 1, wherein the first and second domain configuration information configures the domains for channel decoding transmissions based on different modulation standards;

Claim 20 (new): The multi-processor system of claim 1, wherein the configuration information provided by the global control processor at times configures the first domain processing means and the second domain processing means for channel decoding 8-VSB transmissions based on the ATSC standard.